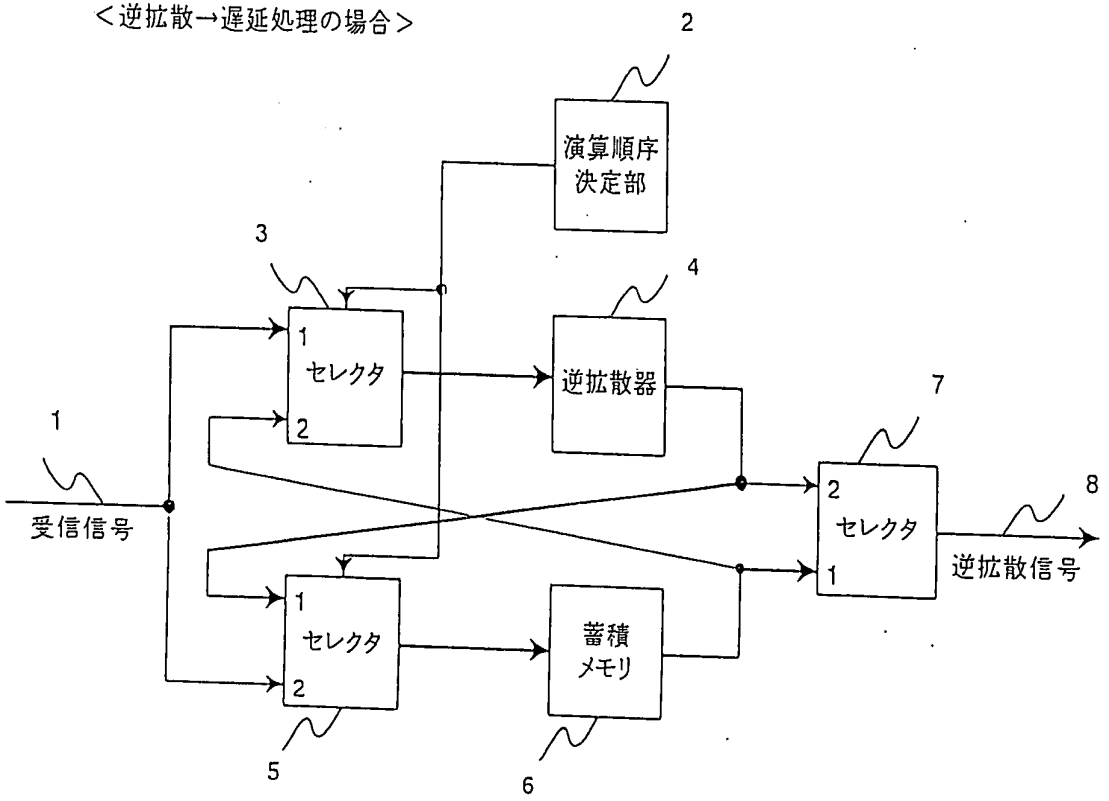


Fig. 1

<Case of reverse diffusion → delay processing>

(1) receiving signal

(2) calculation order determining portion

(3) selector

(4) reverse diffusing unit

(5) selector

(6) storage memory

(7) selector

(8) reverse diffusing signal

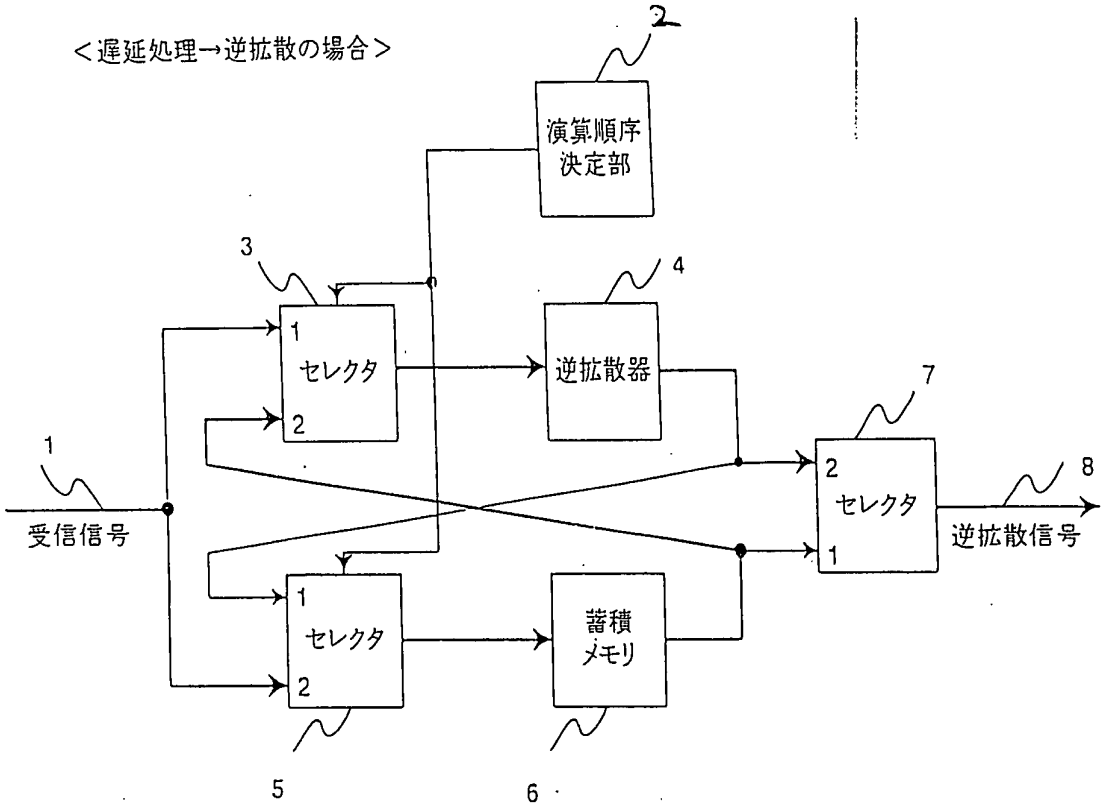


Fig. 2

Fig. 2

<Case of delay processing → reverse diffusion>

(1) receiving signal

(2) calculation order determining portion

(3) selector

(4) reverse diffusing unit

(5) selector

(6) storage memory

(7) selector

(8) reverse diffusing signal

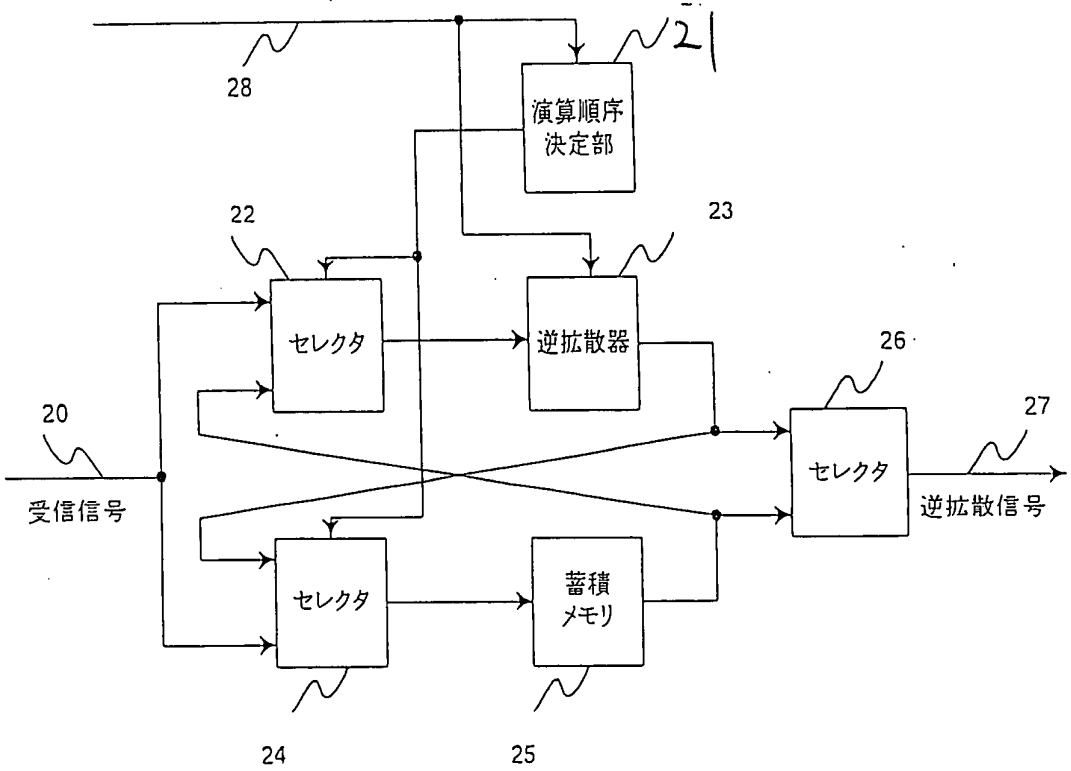


Fig. 3

(20) receiving signal

(21) calculation order determining portion

(22) selector

(23) reverse diffusing unit

(24) selector

(25) storage memory

(26) selector

(27) reverse diffusing signal

(28) symbol rate information

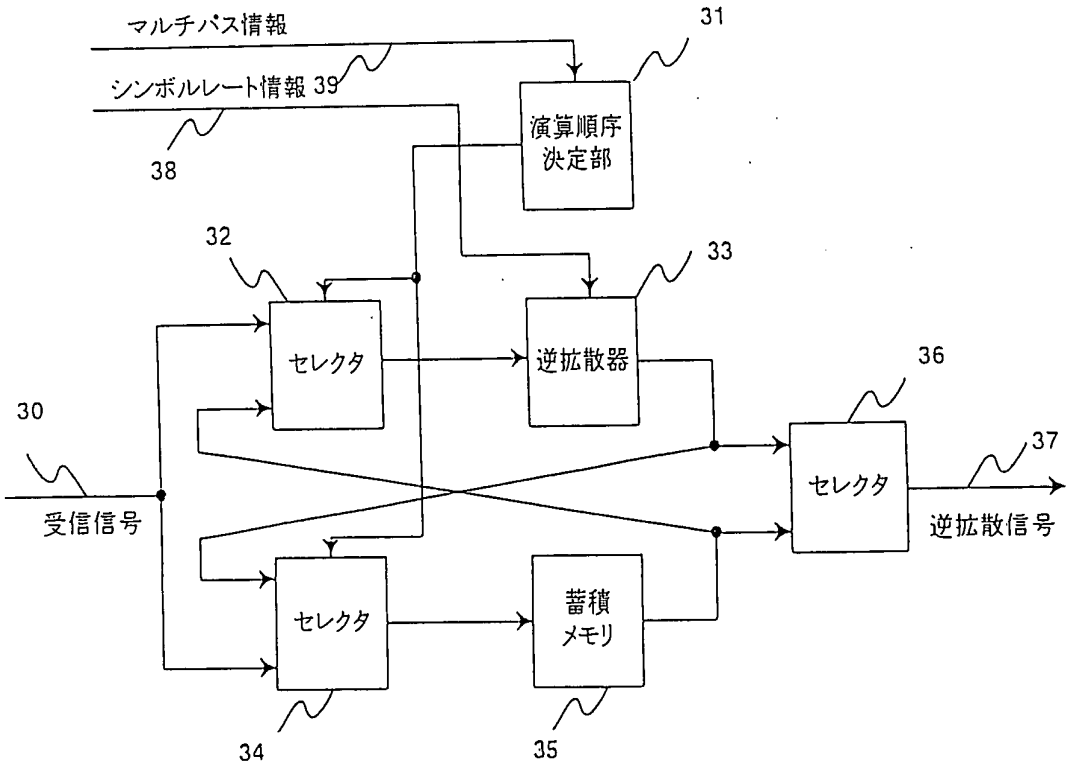


Fig. 4

(30) receiving signal
(31) calculation order determining portion
(32) selector
(33) reverse diffusing unit
(34) selector
(35) storage memory
(36) selector
(37) reverse diffusing signal
(38) symbol rate information
(39) multipass information

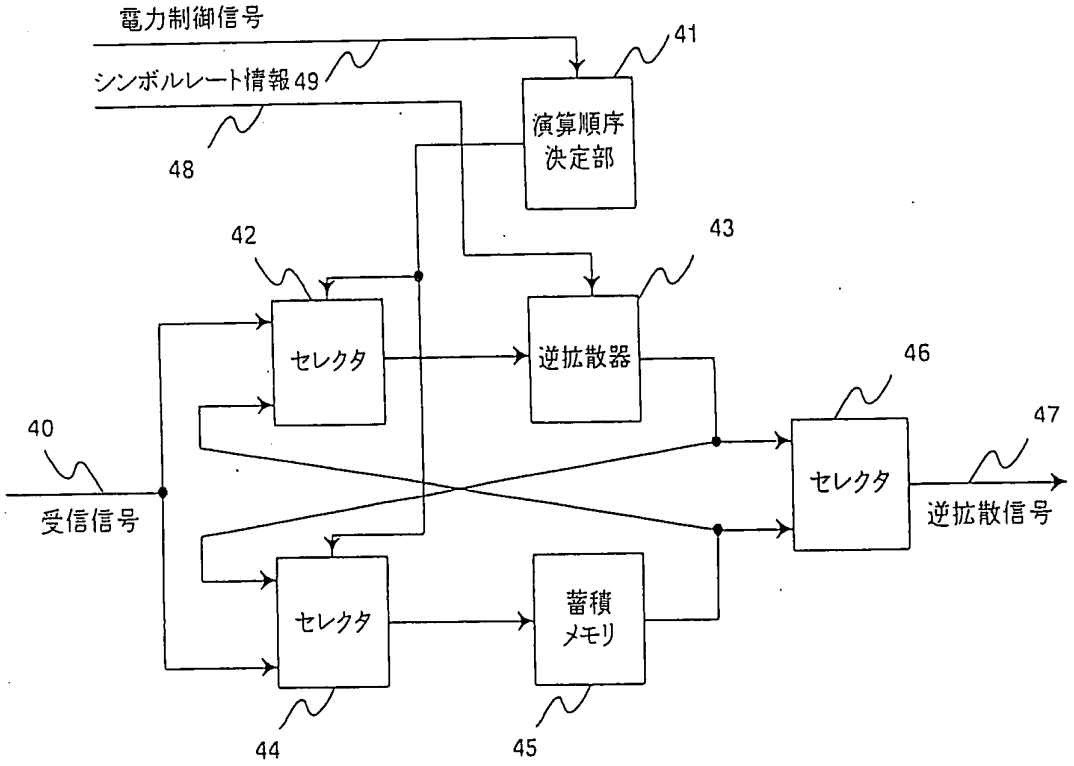


Fig. 5

(40) receiving signal

(41) calculation order determining portion

(42) selector

(43) reverse diffusing unit

(44) selector

(45) storage memory

(46) selector

(47) reverse diffusing signal

(48) symbol rate information

(49) power control signal

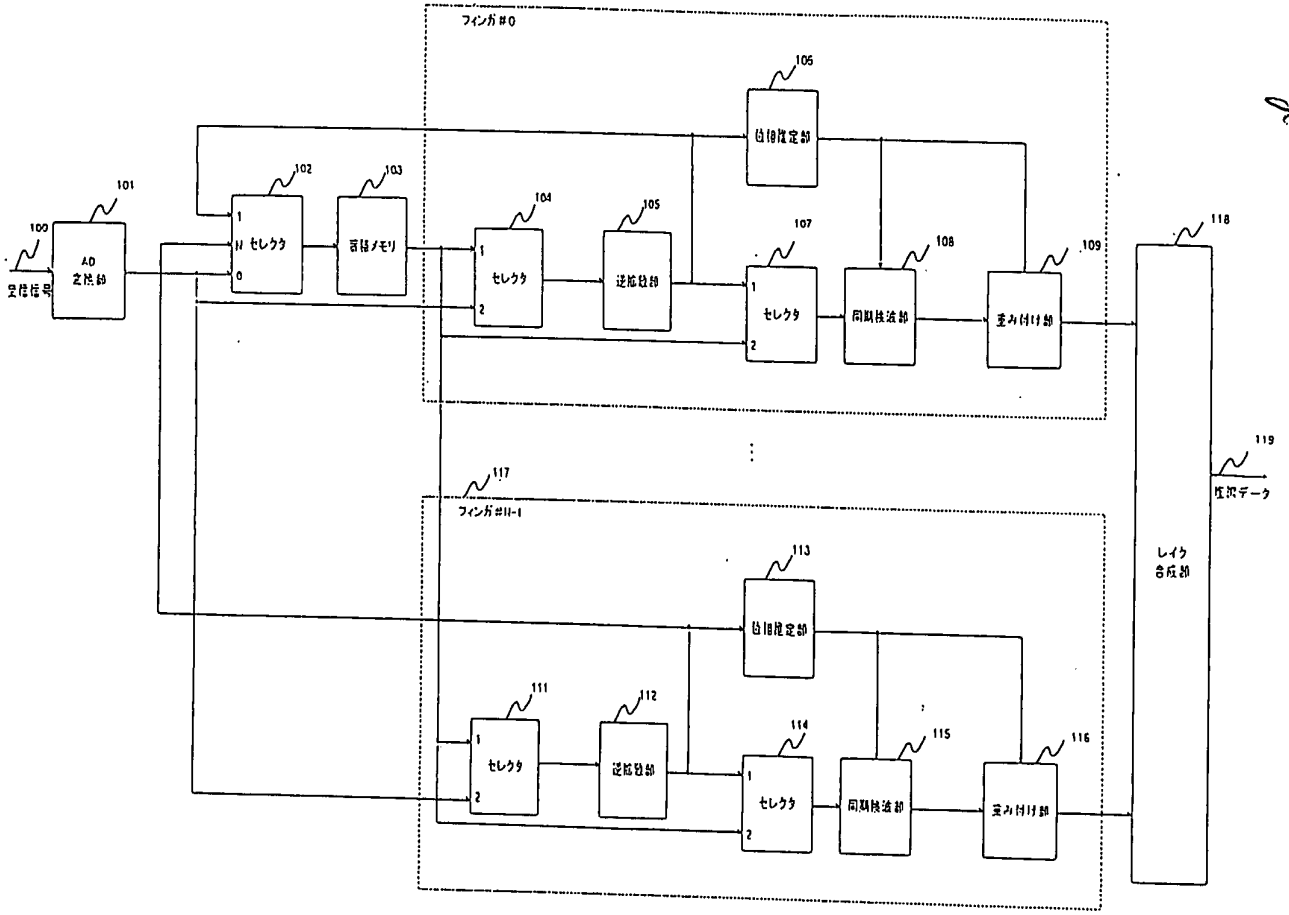


Fig. 6

(100) receiving signal
(101) AD converting portion
(102) selector
(103) storage memory
(104) selector
(105) reverse diffusing portion
(106) phase estimating portion
(107) selector
(108) synchronous detecting portion
(109) weighting portion
(110) finger
(111) selector
(112) reverse diffusing portion
(113) phase estimating portion
(114) selector
(115) synchronous detecting portion
(116) weighting portion
(117) finger
(118) rake synthesizing portion
(119) demodulated data

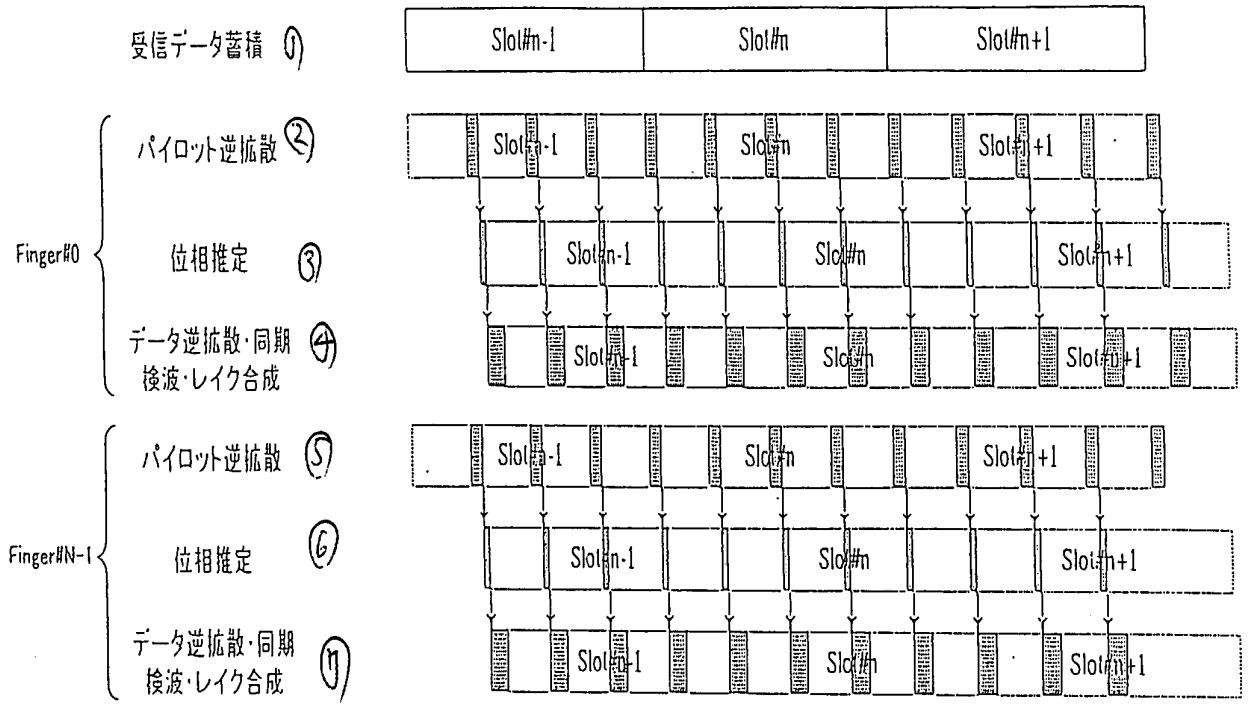
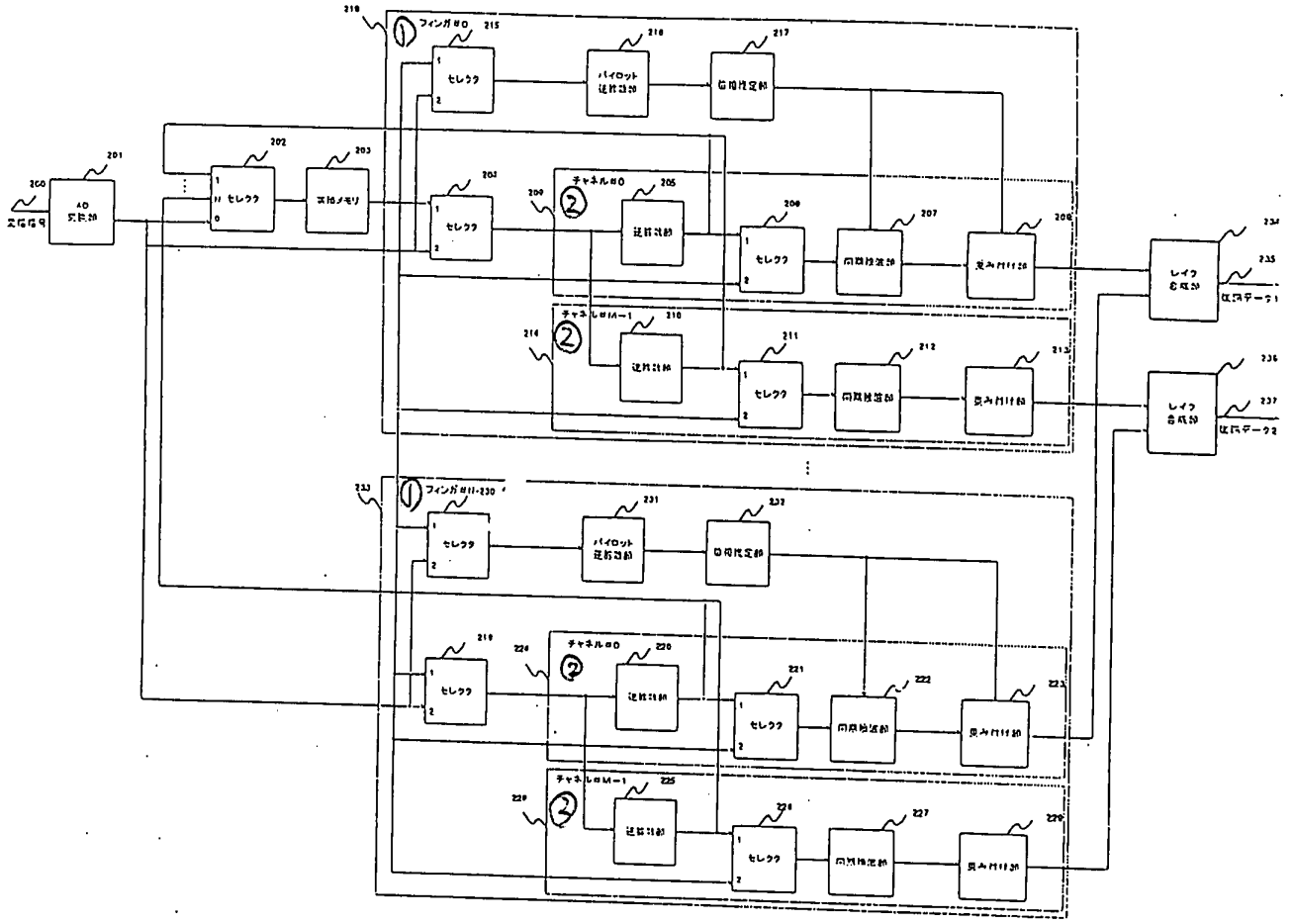


Fig.1

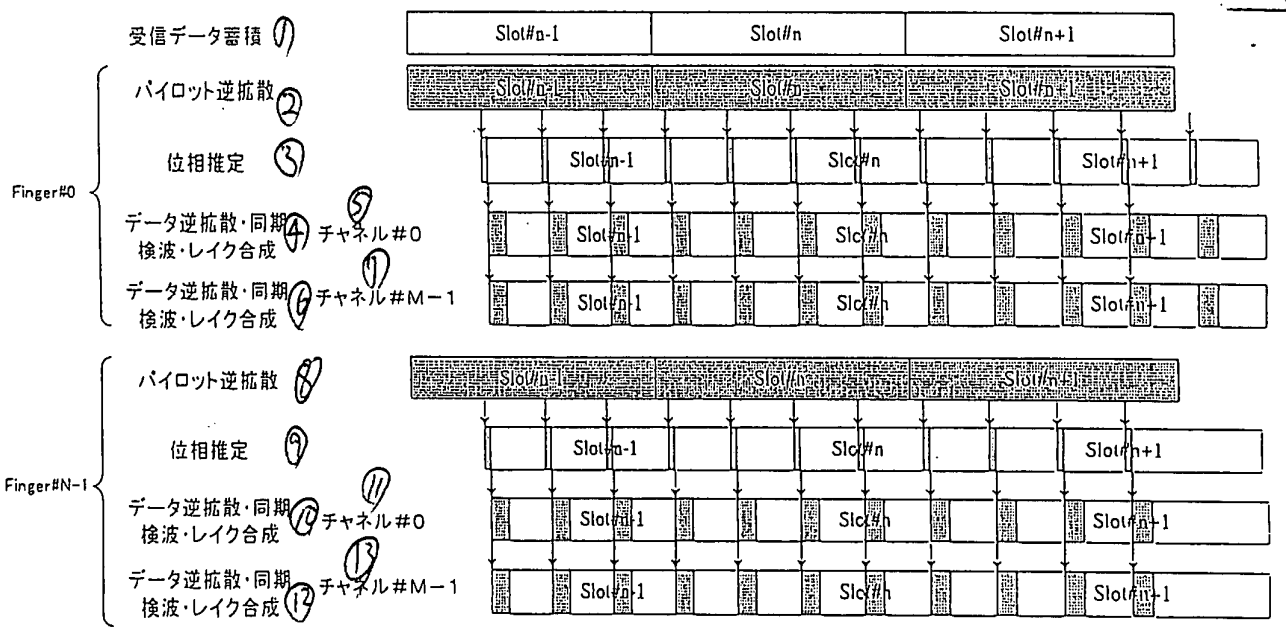
① Receive data storage
② Pilot reverse diffusion
③ Phase estimation
④ Data reverse diffusion □ synchronous detection □ rake synthesis
⑤ Pilot reverse diffusion
⑥ Phase estimation
⑦ Data reverse diffusion □ synchronous detection □ rake synthesis

Fig. 8



(200) receiving signal
(201) AD converting portion
(202) selector
(203) storage memory
(204) selector
(205) reverse diffusing portion
(206) selector
(207) synchronous detecting portion
(208) weighting portion
(210) reverse diffusing portion
(211) selector
(212) synchronous detecting portion
(213) weighting portion
(215) selector
(216) pilot reverse diffusing portion
(217) phase estimating portion
(219) selector
(220) reverse diffusing portion
(221) selector
(222) synchronous detecting portion
(223) weighting portion
(225) reverse diffusing portion
(226) selector
(227) synchronous detecting portion
(228) weighting portion
(234) rake synthesizing portion
(235) demodulated data
(236) rake synthesizing portion
(237) demodulated data
Finger (1)
Channel (2)

Fig. 9



① Receive data storage
② Pilot reverse diffusion
③ Phase eslimation
④ Data reverse diffusion □ synchronous detection □ rake synthesis
⑤ Channel
⑥ Data reverse diffusion □ synchronous detection □ rake synthesis
⑦ Channel
⑧ Pilot reverse diffusion
⑨ Phase estimation
⑩ Data reverse diffusion □ synchronous detection □ rake synthesis
⑪ Channel
⑫ Data reverse diffusion □ synchronous detection □ rake synthesis
⑬ Channel

Fig. 10

(300) receiving signal
(301) AD converting portion
(302) selector
(303) storage memory
(304) selector
(305) reverse diffusing portion
(306) selector
(307) synchronous detecting portion
(309) weighting portion
(311) selector
(312) pilot reverse diffusing portion
(313) phase estimating portion
(315) selector
(316) reverse diffusing portion
(317) selector
(318) synchronous detecting portion
(319) weighting portion
(321) selector
(322) pilot reverse diffusing portion
(323) phase estimating portion
(325) rake synthesizing portion
(326) demodulated data
(327) demodulated data
Finger (1)
Channel (2)

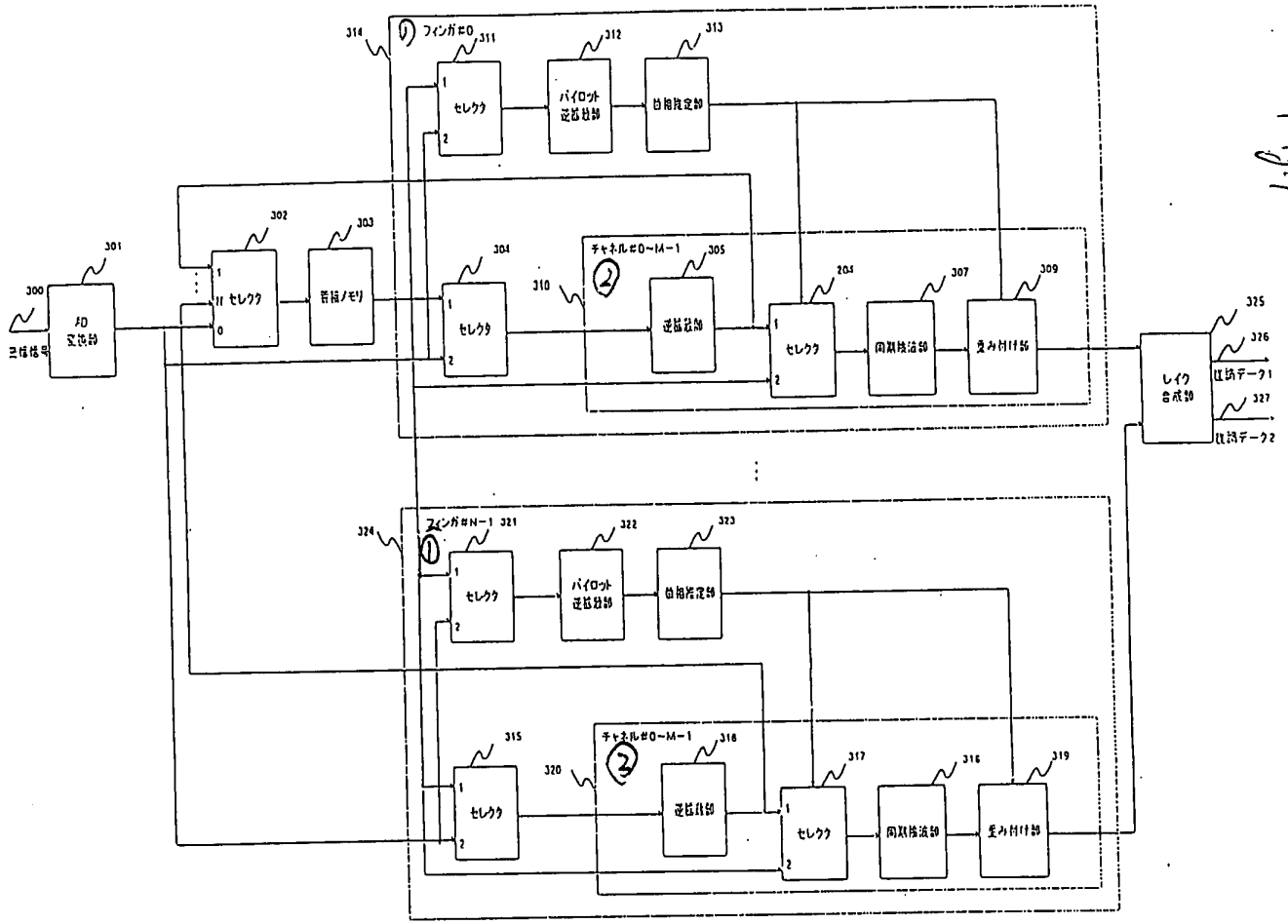
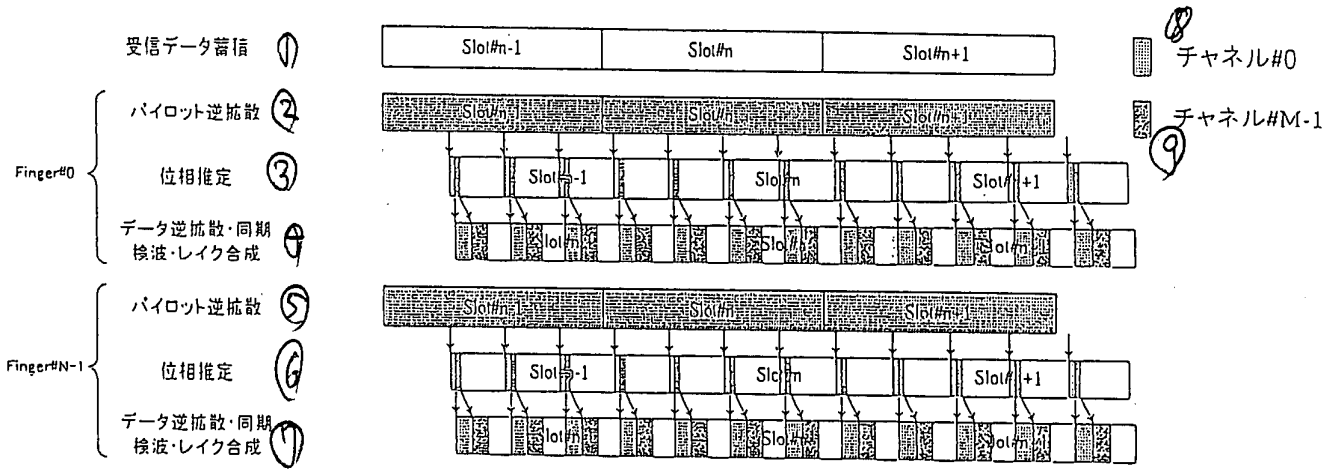


Fig.1



① Receive data storage
② Pilot reverse diffusion
③ Phase estimation
④ Data reverse diffusion □ synchronous detection □ rake synthesis
⑤ Pilot reverse diffusion
⑥ Phase estimation
⑦ Data reverse diffusion □ synchronous detection □ rake synthesis
⑧ Channel
⑨ Channel

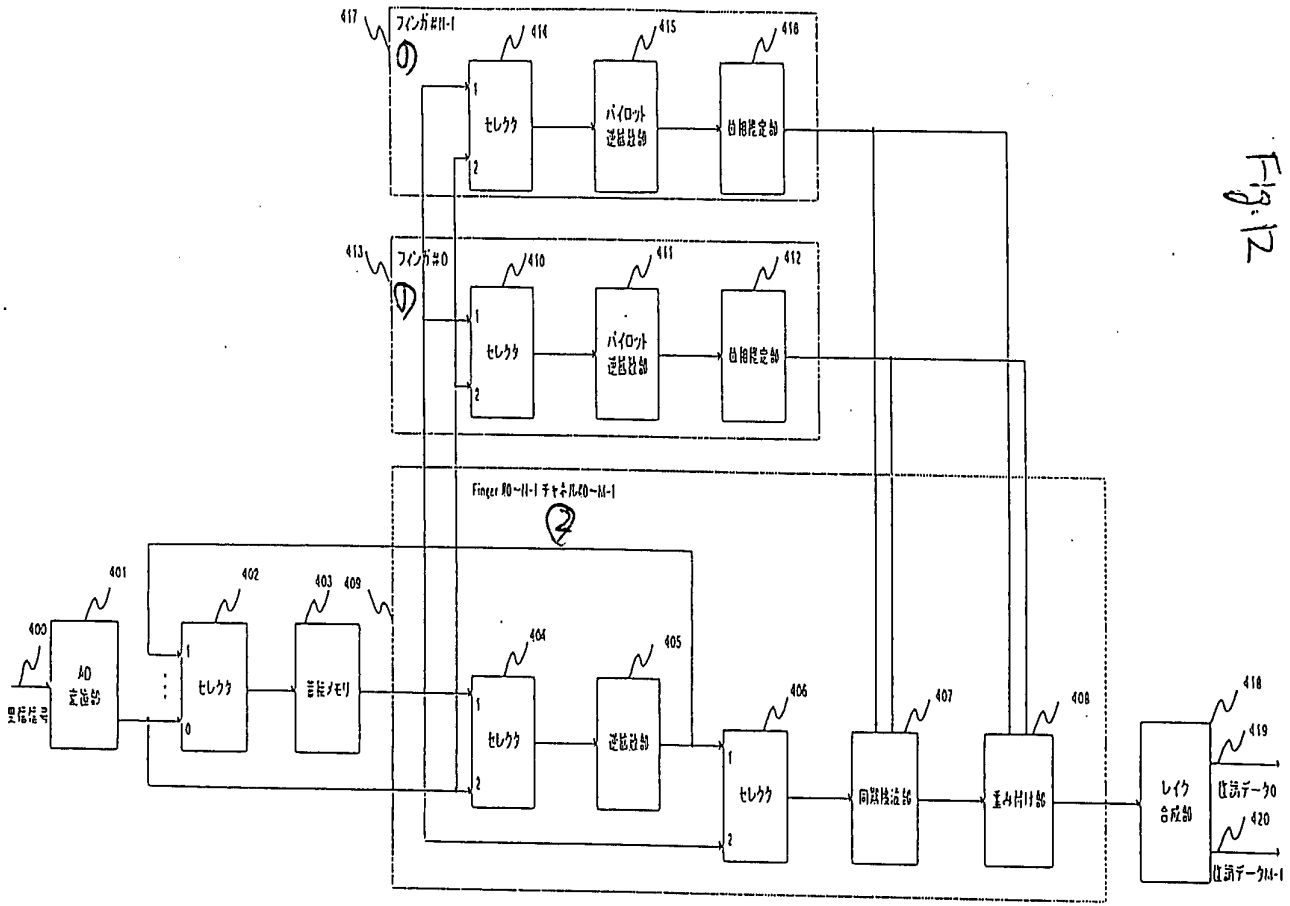


Fig. 12

(400) receiving signal
(401) AD converting portion
(402) selector
(403) storage memory
(404) selector
(405) reverse diffusing portion
(406) selector
(407) synchronous detecting portion
(408) weighting portion
(410) selector
(411) pilot reverse diffusing portion
(412) phase estimating portion
(414) selector
(415) pilot reverse diffusing portion
(416) phase estimating portion
(418) rake synthesizing portion
(419) demodulated data
(420) demodulated data

① Finger

|

② Channel

Fig 13

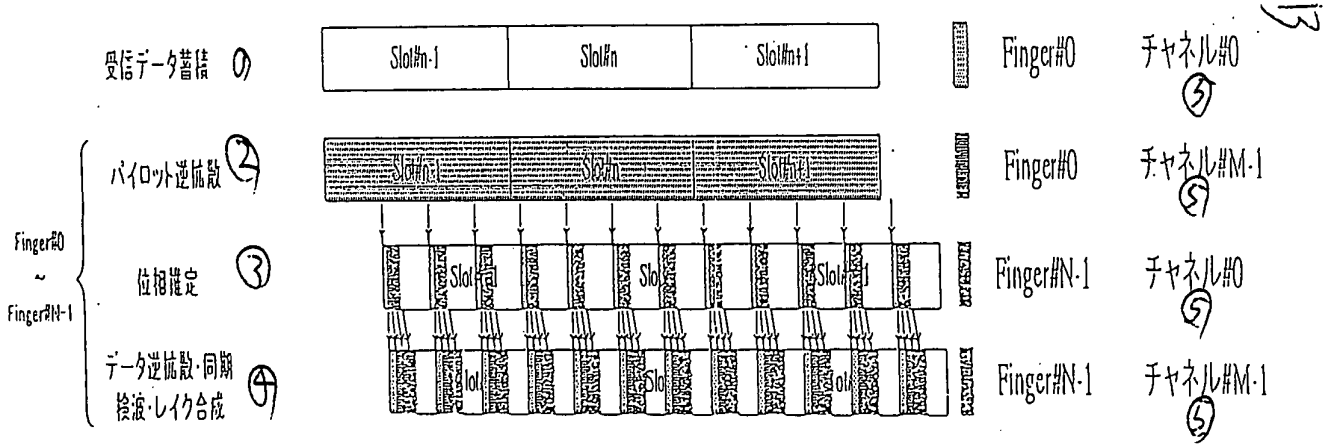


Fig. 13

① Receive data storage

② Pilot reverse diffusion

③ Phase estimation

④ Data reverse diffusion □ synchronous detection □ rake synthesis

⑤ Channel

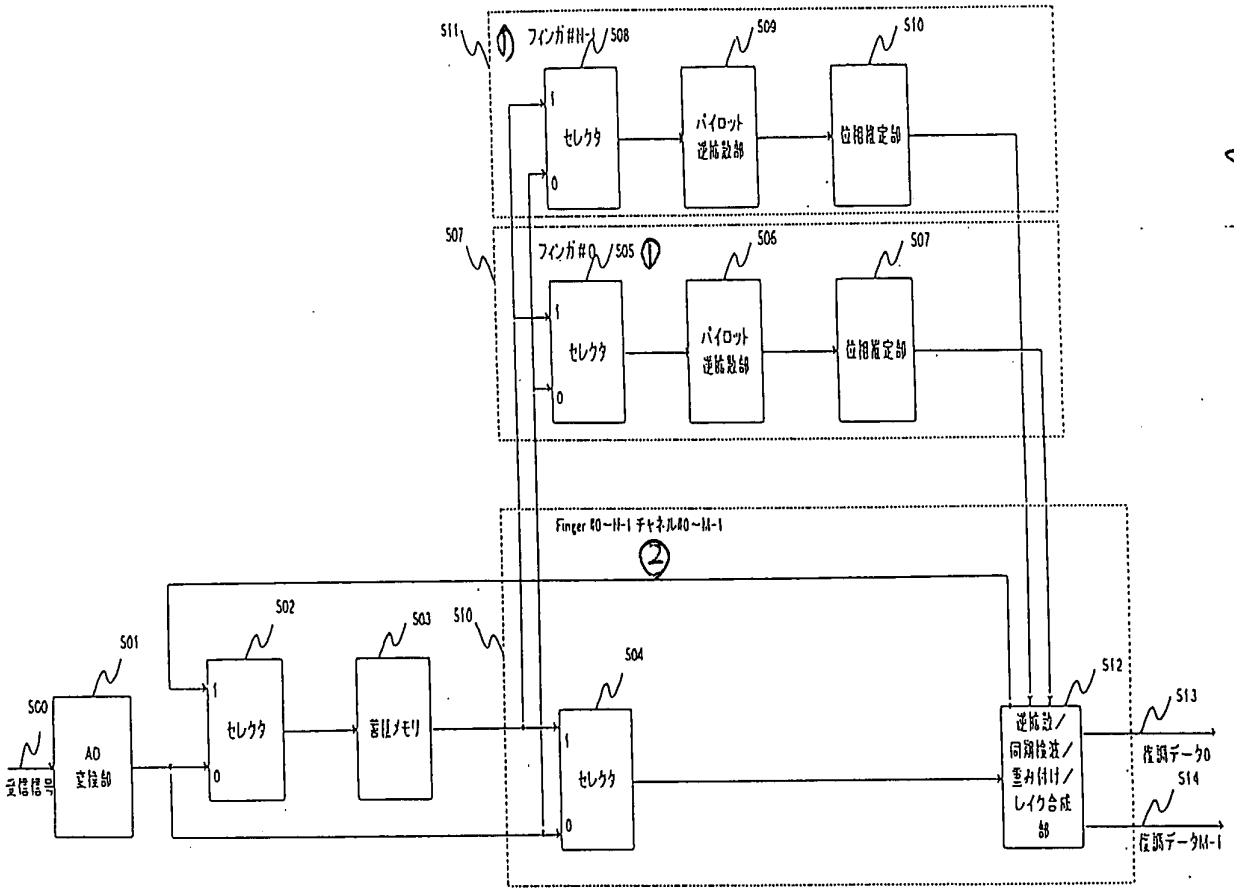


Fig. 14

(500) receiving signal

(501) AD converting portion

(502) selector

(503) storage memory

(504) selector

(505) selector

(506) pilot reverse diffusing portion

(507) phase estimating portion

(508) selector

(509) pilot reverse diffusing portion

(510) phase estimating portion

(512) reverse diffusing / synchronous detecting / weighting / rake synthesizing portion

(513) demodulated data

(514) demodulated data

Finger ①

Channel ②

Fig 14

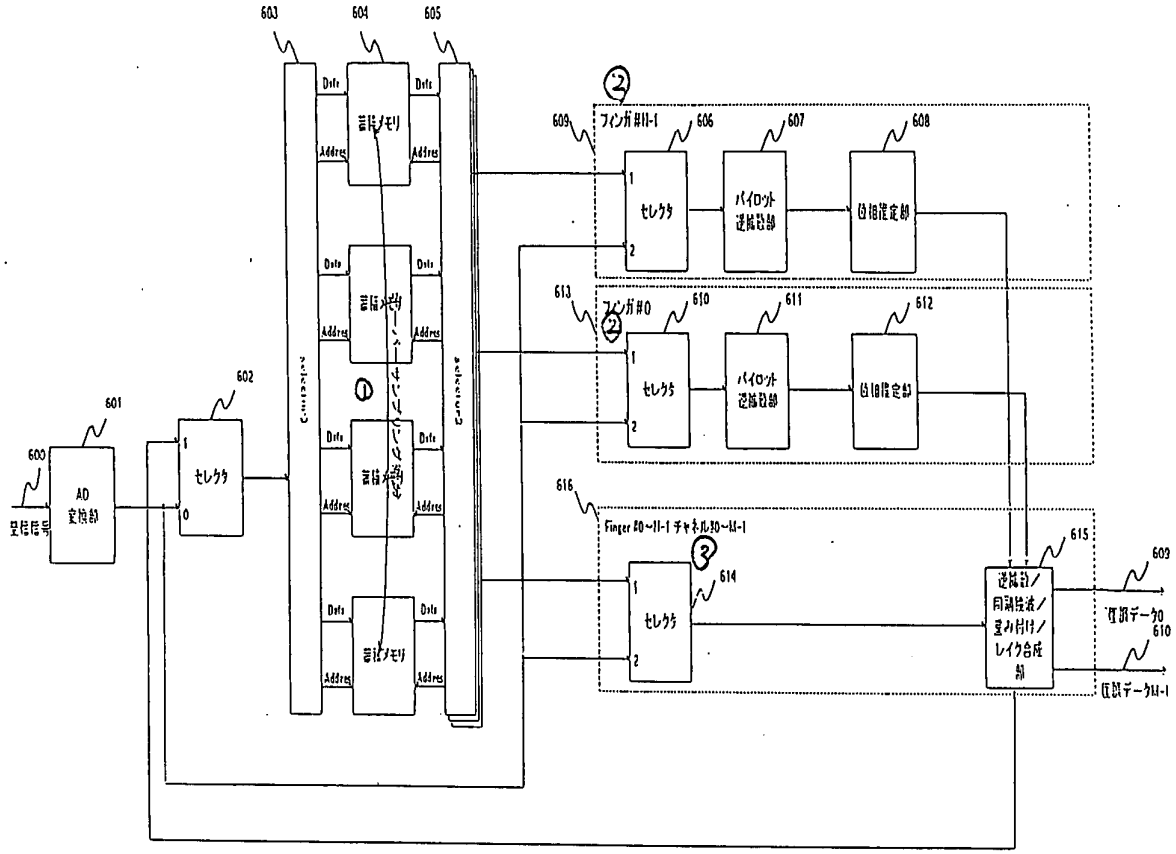


Fig. 15

(600) receiving signal

(601) AD converting portion

(602) selector

(604) storage memory

(606) selector

(607) pilot reverse diffusing portion

(608) phase estimating portion

(609) demodulated data

(610) demodulated data

(610) selector

(611) pilot reverse diffusing portion

(612) phase estimating portion

(614) selector

(615) reverse diffusing / synchronous detecting / weighting / rake synthesizing portion

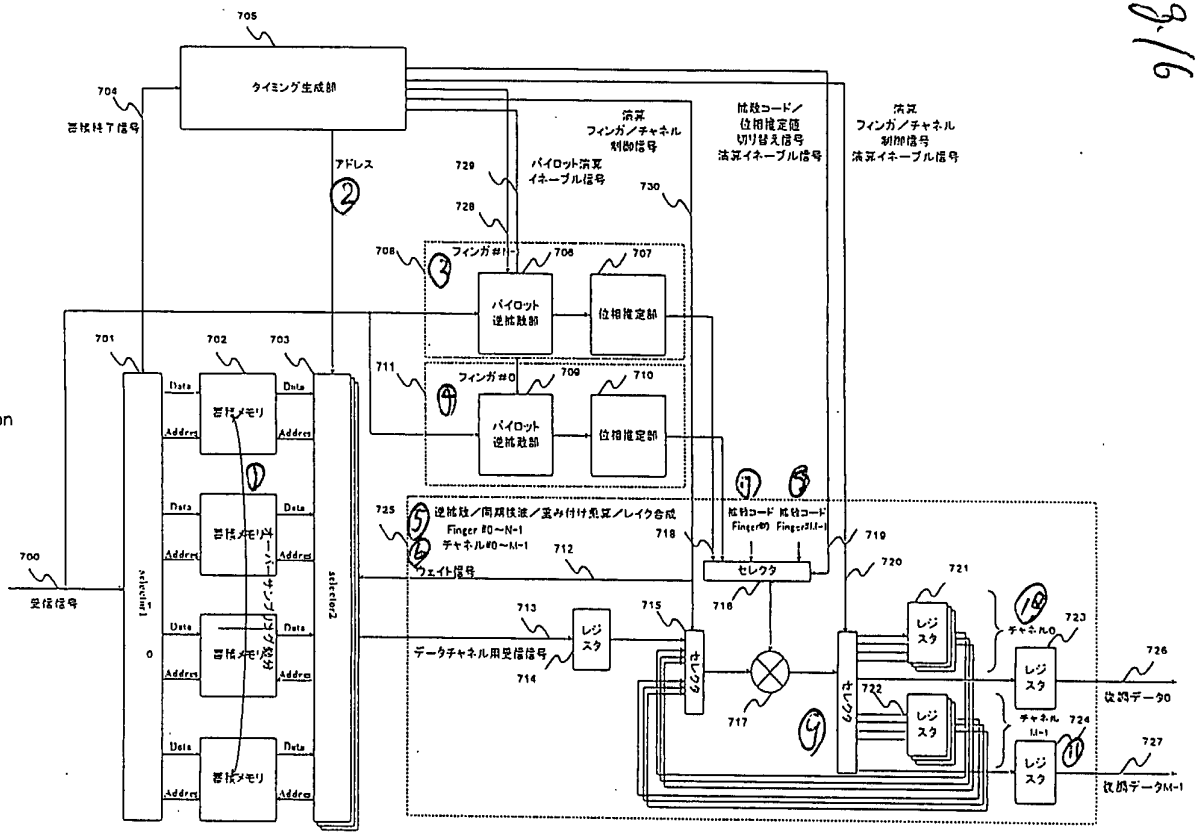
Portion of oversampling number ①

Finger ②

Channel ③

Fig 15

(700) receiving signal
(702) storage memory
(704) storage end signal
(705) timing generating portion
(706) pilot reverse diffusing portion
(707) phase estimating portion
(709) pilot reverse diffusing portion
(710) phase estimating portion
(712) wait signal
(713) receiving signal for data channel
(714) register
(715) selector
(716) selector
(719) diffusion code / phase estimation value / switching signal / calculation enable signal
(720) Calculation finger / channel control signal calculation enable signal
(721) register
(722) register
(723) register
(724) register
(726) demodulated data
(727) demodulated data
(729) pilot calculation enable signal
(730) calculation finger / channel control signal
Portion of oversampling number (1)
Address (2)
Finger (3)
Finger (9)



(5) Reverse diffusion / synchronous detection / weighting multiplication / rake synthesis
(6) Channel
(7) Diffusion code
(8) Diffusion code
(9) Selector
(10) Channel
(11) Channel

Fig. 9/9

Fig. 17

① Receiving signal for data channel
② Calculation (reverse diffusion / synchronous detection / rake synthesis)
③ Wait signal
④ Calculation enable signal
⑤ Calculation enable signal
⑥ Synchronous detection
⑦ Synchronous detection
⑧ Synchronous detection
⑨ Synchronous detection
⑩ Rake synthesis

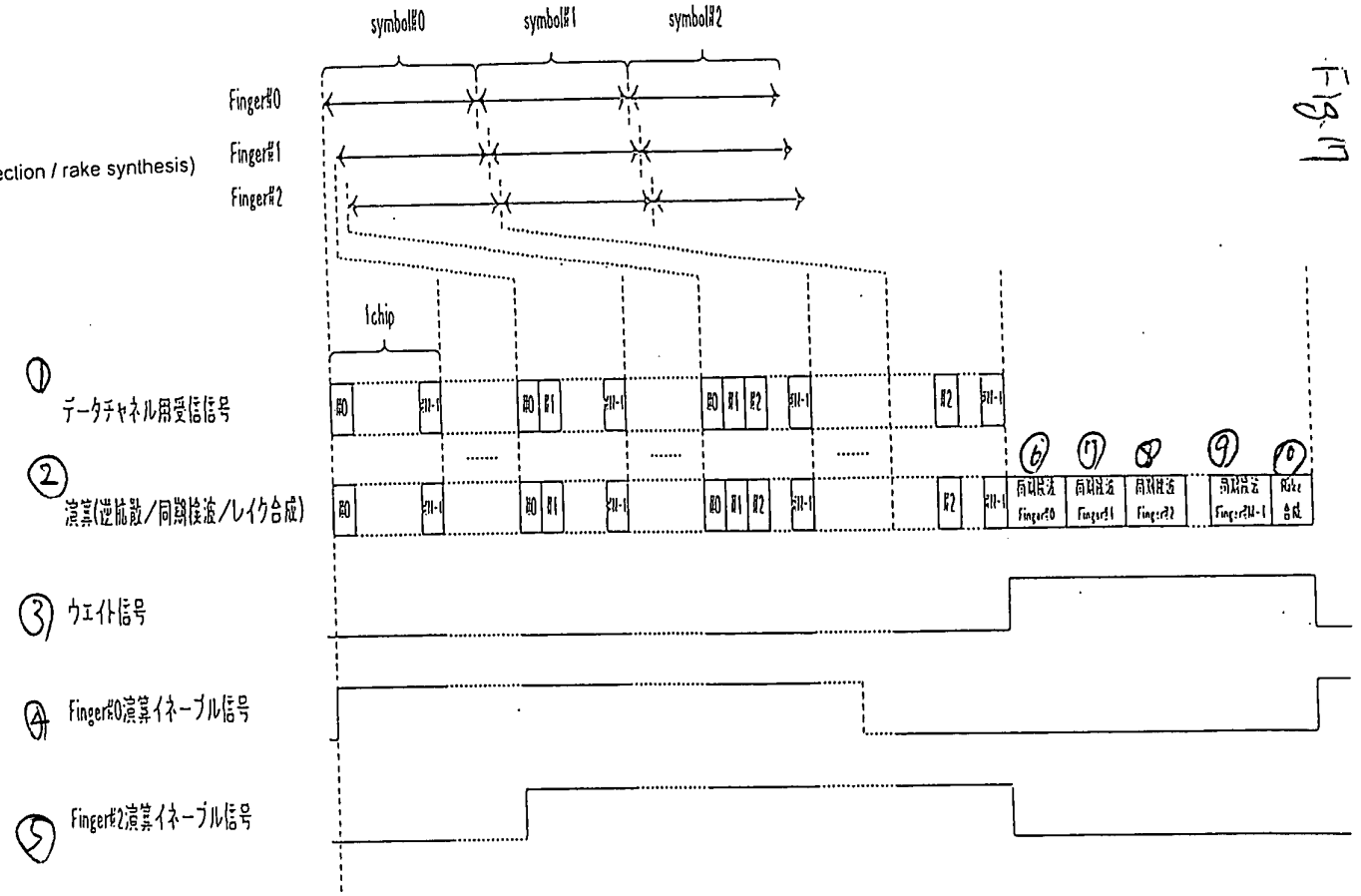


Fig. 17

Fig. 18

(800) receiving signal

(802) storage memory

(804) storage end signal

(805) liming generating portion

(806) pilot reverse diffusing portion

(807) phase estimating portion

(809) pilot reverse diffusing portion

(810) phase estimating portion

(812) receiving signal for data channel

(813) register

(814) selector

(815) selector

(818) diffusion code / phase estimation value switching signal

(819) calculation finger / channel control signal

(820) register

(821) register

(822) register

(823) register

(825) demodulated data

(826) demodulated data

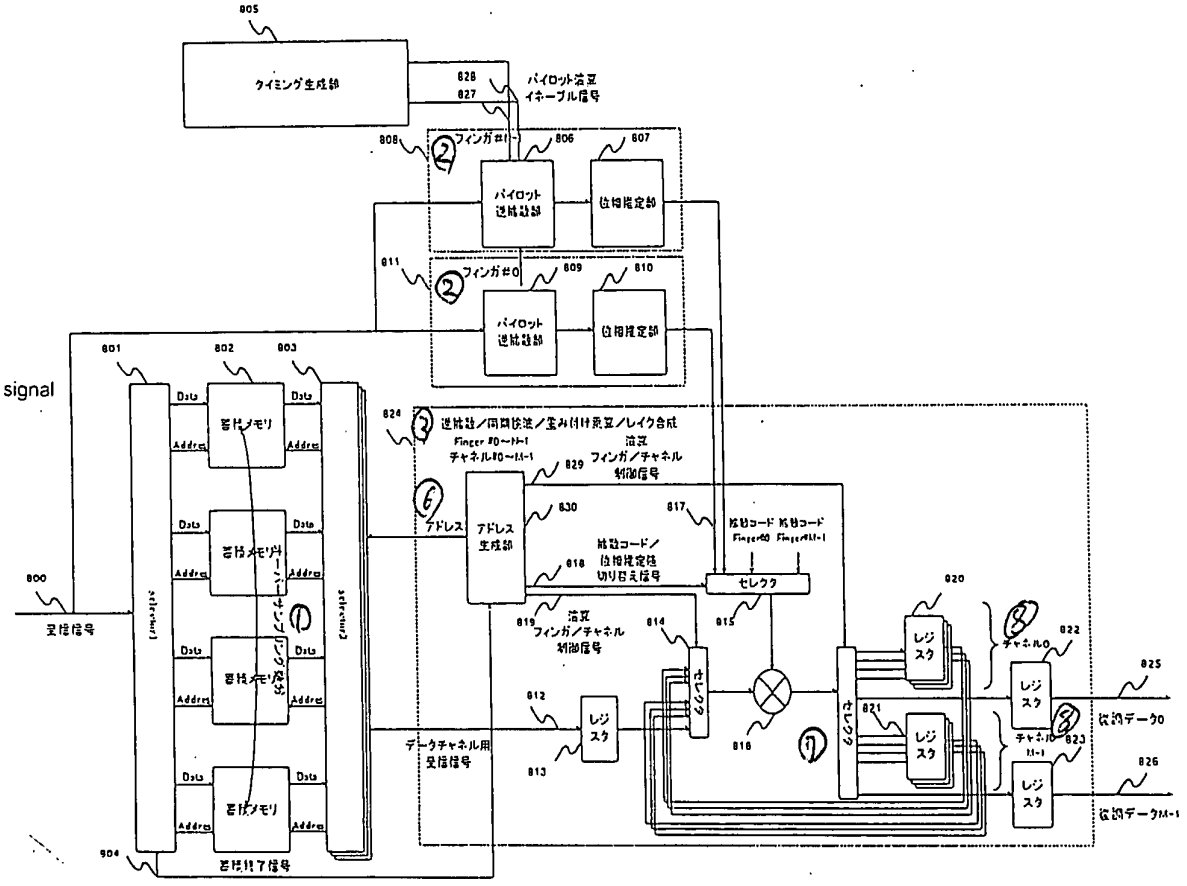
(828) pilot calculation enable signal

(829) calculation finger / channel control signal

(830) address generating portion

① Portion of oversampling number

② Finger



③ Reverse diffusion / synchronous detection / weighting multiplication / rake synthesis

④ Channel

⑤ Address

⑥ Diffusion code

⑦ Selector

⑧ Channel

Fig. 19

① Receiving signal for data channel
② Calculation (reverse diffusion / synchronous detection / rake synthesis)
③ Calculation enable signal
④ Calculation enable signal
⑤ Synchronous detection
⑥ Synchronous detection
⑦ Synchronous detection
⑧ Synchronous detection
⑨ Rake synthesis

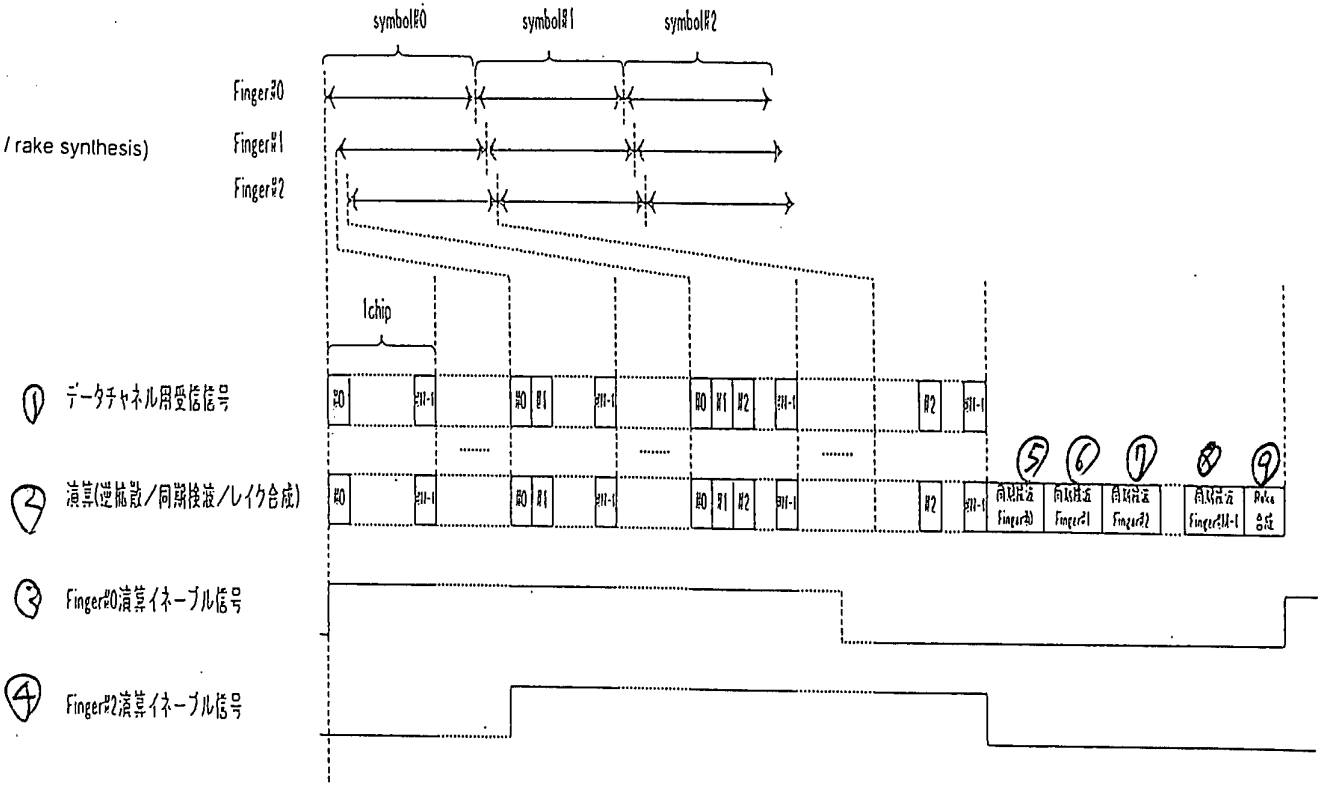


Fig. 26

(800) receiving signal
(802) storage memory
(804) storage end signal
(805) timing generating portion
(806) pilot reverse diffusing portion
(807) phase estimating portion
(809) pilot reverse diffusing portion
(810) phase estimating portion
(812) receiving signal for data channel
(813) register
(814) selector
(815) selector
(818) diffusion code / phase estimation value switching signal
(819) calculation finger / channel control signal
(820) register
(821) register
(822) register
(823) register
(825) demodulated data
(826) demodulated data
(827) address / timing / calculating procedure storage device
(828) pilot calculation enable signal
(829) calculation finger / channel control signal
(830) address generating portion
(11) Portion of oversampling number
(1) Finger
(2) Reverse diffusion / synchronous detection / weighting multiplication / rake synthesis
(2) Channel
(4) Address
(5) Diffusion code
(6) Selector

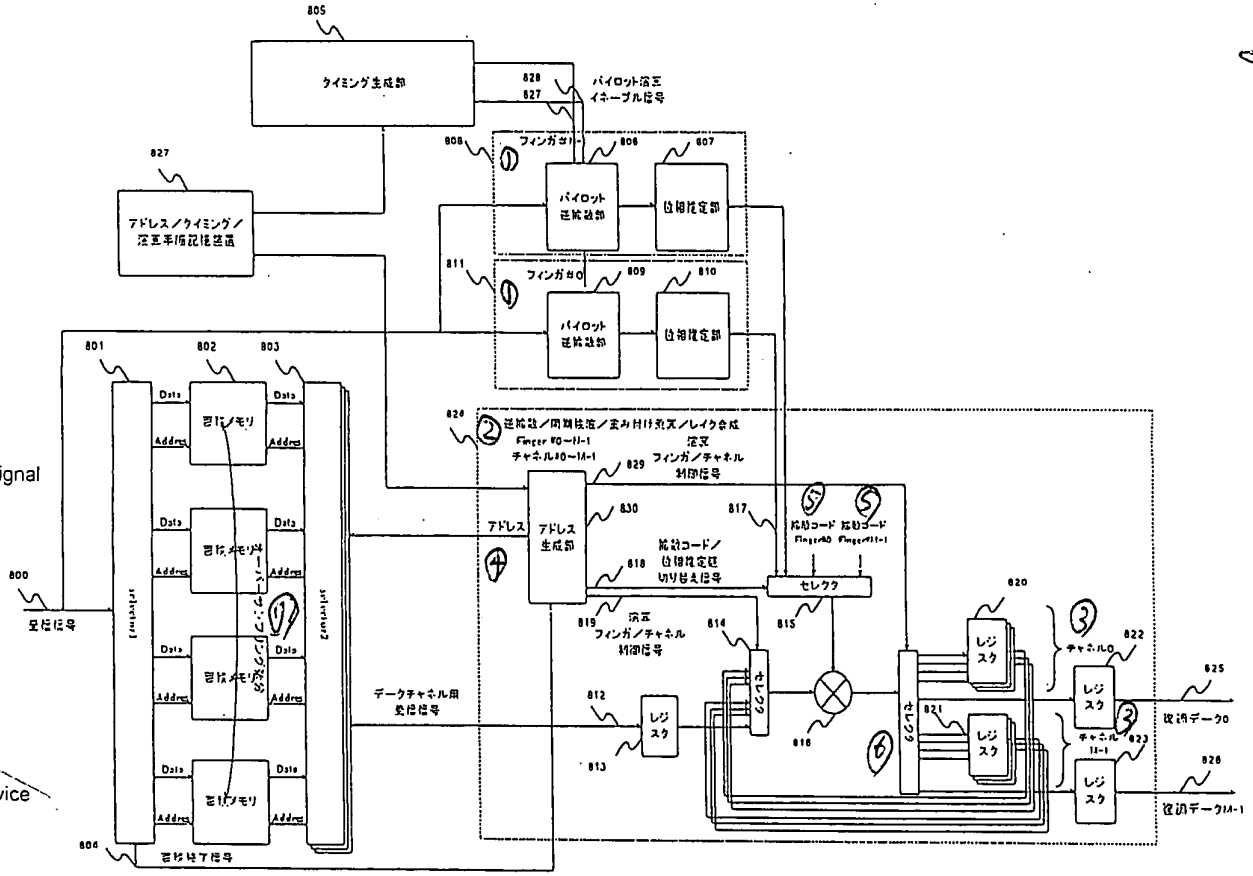
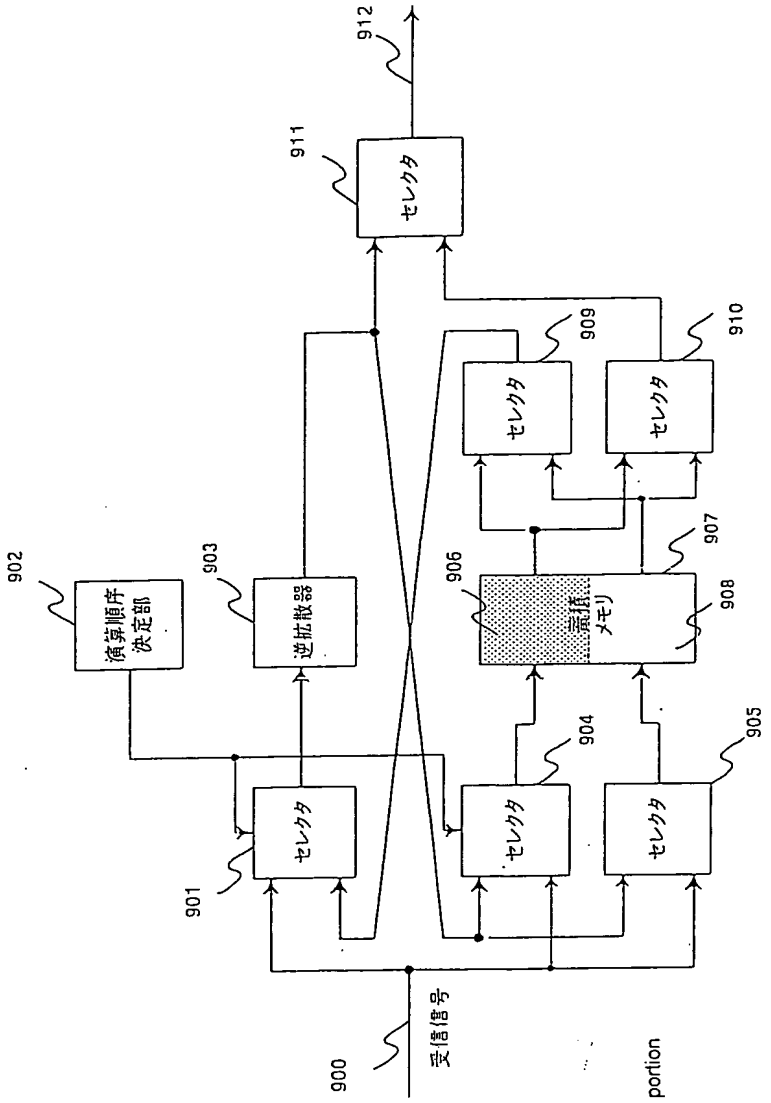


Fig 21



(900) receiving signal
(901) selector
(902) calculation order determining portion
(903) reverse diffusing unit
(904) selector
(905) selector
(907) storage memory
(909) selector
(910) selector
(911) selector

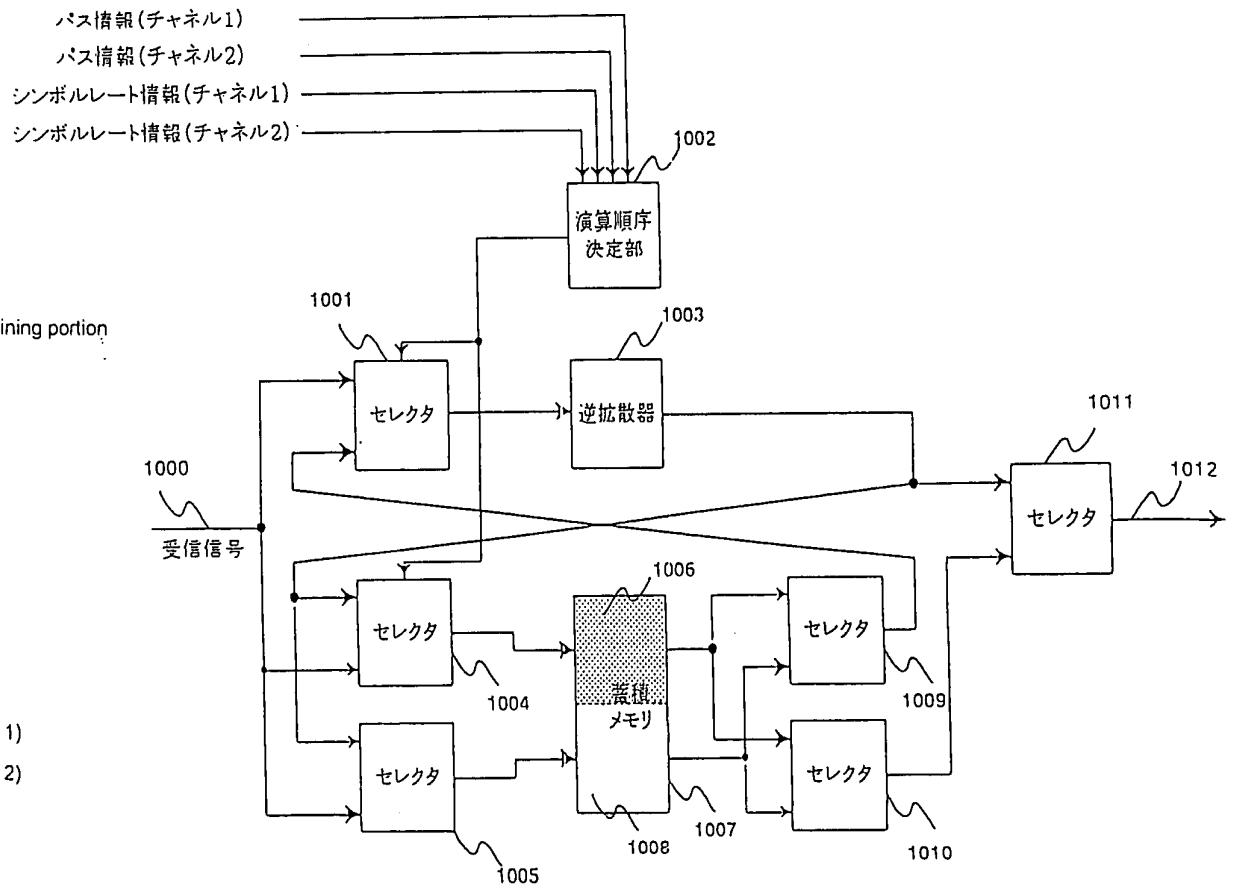


Fig. 22

(1000). receiving signal

(1001) selector

(1002) calculation order determining portion

(1003) reverse diffusing unit

(1004) selector

(1005) selector

(1007) storage memory

(1009) selector

(1010) selector

(1011) selector

Pass information (channel 1)

Pass information (channel 2)

Symbol rate information (channel 1)

Symbol rate information (channel 2)

Fig. 22

Fig.23

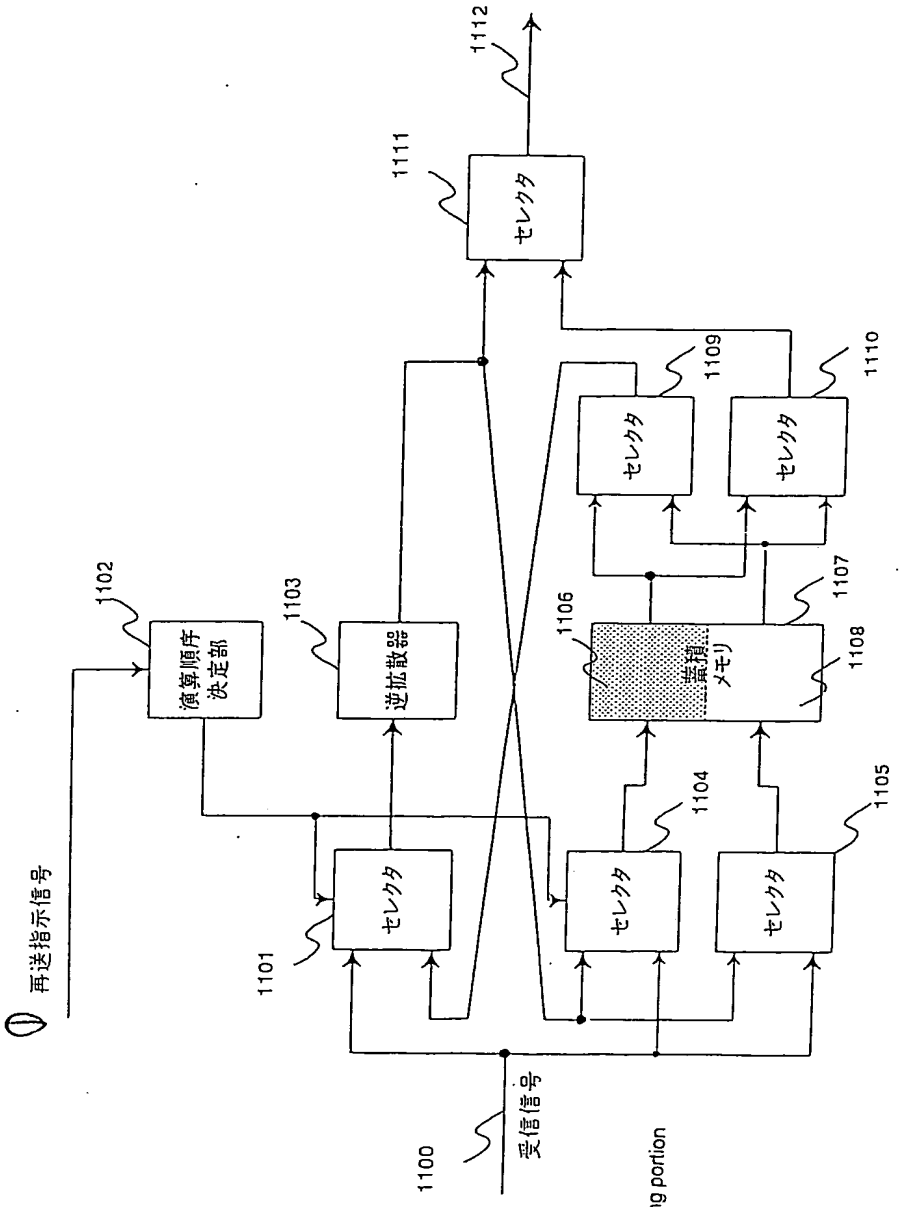


Fig. 23
(1100) receiving signal
(1101) selector
(1102) calculation order determining portion
(1103) reverse diffusing unit
(1104) selector
(1105) selector
(1107) storage memory
(1109) selector
(1110) selector
(1111) selector
Retransmission indicating signal ①

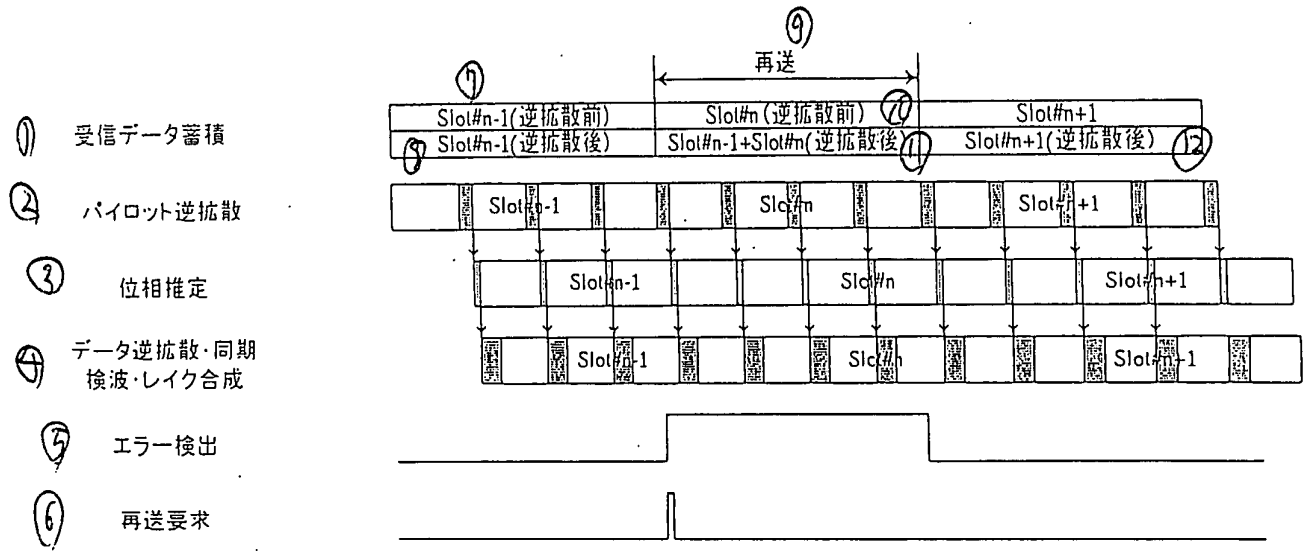


Fig. 24

Fig. 24

⑨ Receive data storage
② Pilot reverse diffusion
③ Phase estimation
④ Data reverse diffusion □ synchronous detection □ rake synthesis
⑤ Error detection
⑥ Retransmission request
⑦ Before reverse diffusion
⑧ After reverse diffusion
⑨ Retransmission
⑩ Before reverse diffusion
⑪ After reverse diffusion
⑫ After reverse diffusion

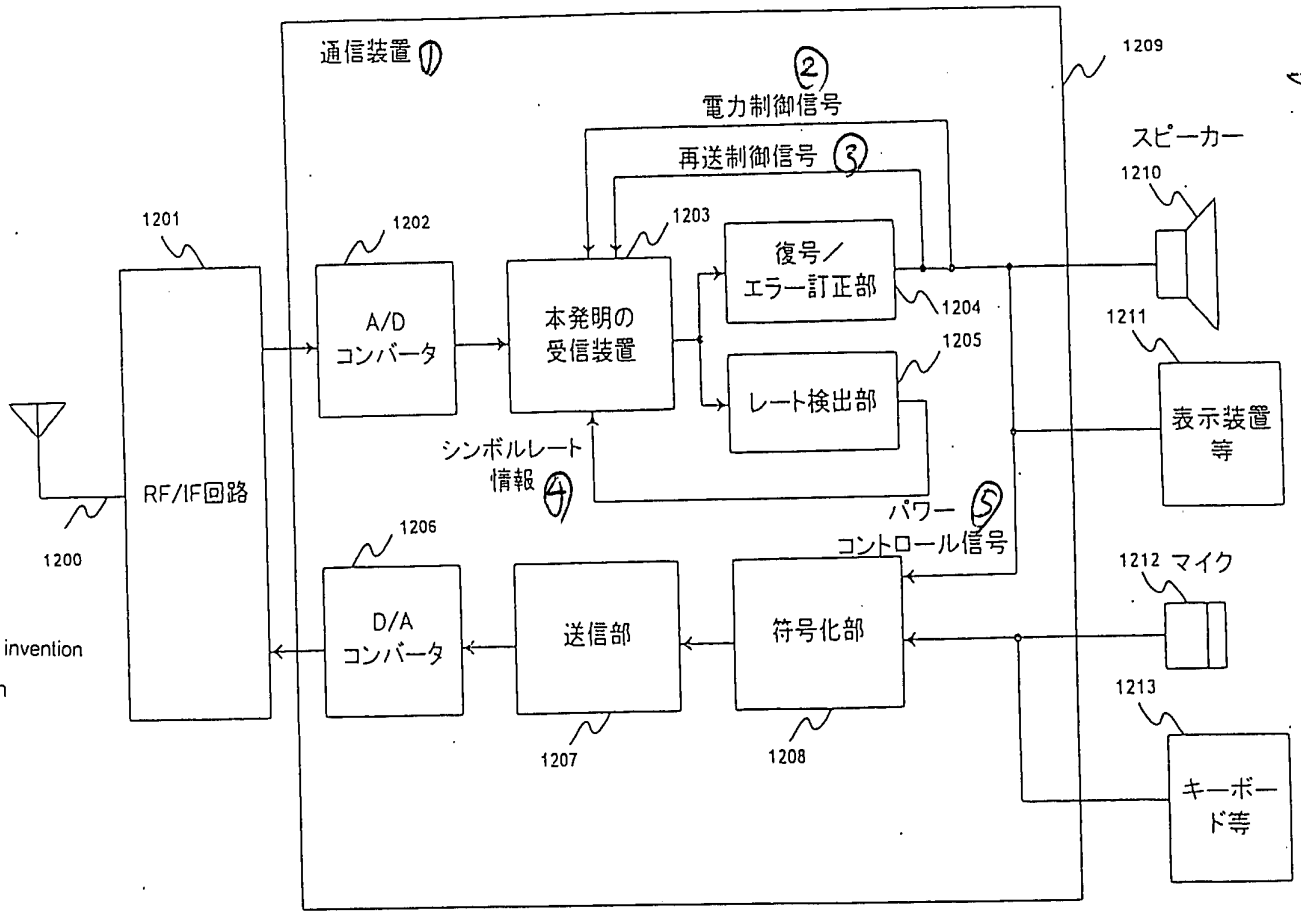


Fig. 25

(1201) RF/IF circuit

(1202) A/D converter

(1203) receiving device according to the invention

(1204) decoding / error correcting portion

(1205) rate detecting portion

(1206) D/A converter

(1207) transmitting portion

(1208) coding portion

(1210) speaker

(1211) display device

(1212) microphone

(1213) keyboard

① Communicating device

② Power control signal

③ Retransmission control signal

④ Symbol rate information

⑤ Power control signal

Fig. 26

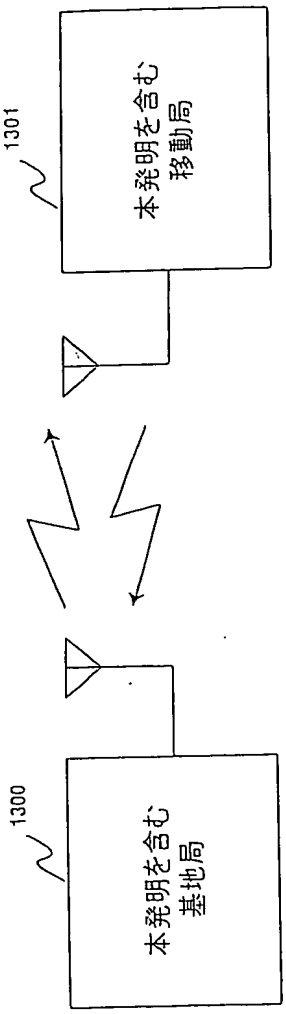


Fig. 26

(1300) base station including the invention

(1301) mobile station including the invention

Fig.27

<Condition>

1. W-CDMA method
2. Number of channels 15
3. Number of receive data bits 6
4. Number of finger passes 12
5. Storage time 1 slot
6. Diffusion rate 4
7. Total number of bits of memory
8. Case of symbol buffer after reverse diffusion
9. Number of input bits
10. Amplification increase rate by reverse diffusion
11. Number of finger passes
12. Number of symbols in slot
13. Number of channels
14. 144000 bits
15. Case of receive data buffer
16. Number of input bits
17. Number of samples in slot
18. 122880 bits

<条件>
・W－CDMA方式 (1)
・チャネル数15 (2)
・受信データビット数6 (3)
・フィンガパス数12 (4)
・蓄積時間1スロット (5)
・拡散率4 (6)

	逆拡散後シンボルバッファの場合 (8)	受信データバッファの場合 (15)
メモリ総ビット数 (7)	6(入力bit数) (9) ×5(逆拡散による振幅増加率) (10) ×12(フィンガパス数) (11) ×(2560／16)(スロット内シンボル数) (12) ×15(チャネル数) (13) ×2(IQ) ＝144000ビット (14)	6(入力bit数) (16) ×(2560×4)(スロット内サンプル数) (17) ×2(IQ) ＝122880ビット (18)

Fig.28

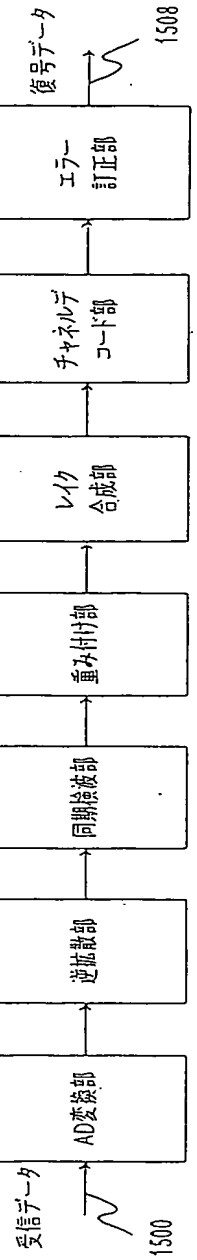


Fig. 28

(1500) Receive data
(1501) AD converting portion
(1502) reverse diffusing portion
(1503) synchronous detecting portion
(1504) weighling portion
(1505) rake synthesizing portion
(1506) channel decoding portion
(1507) error correcting portion
(1508) decode data

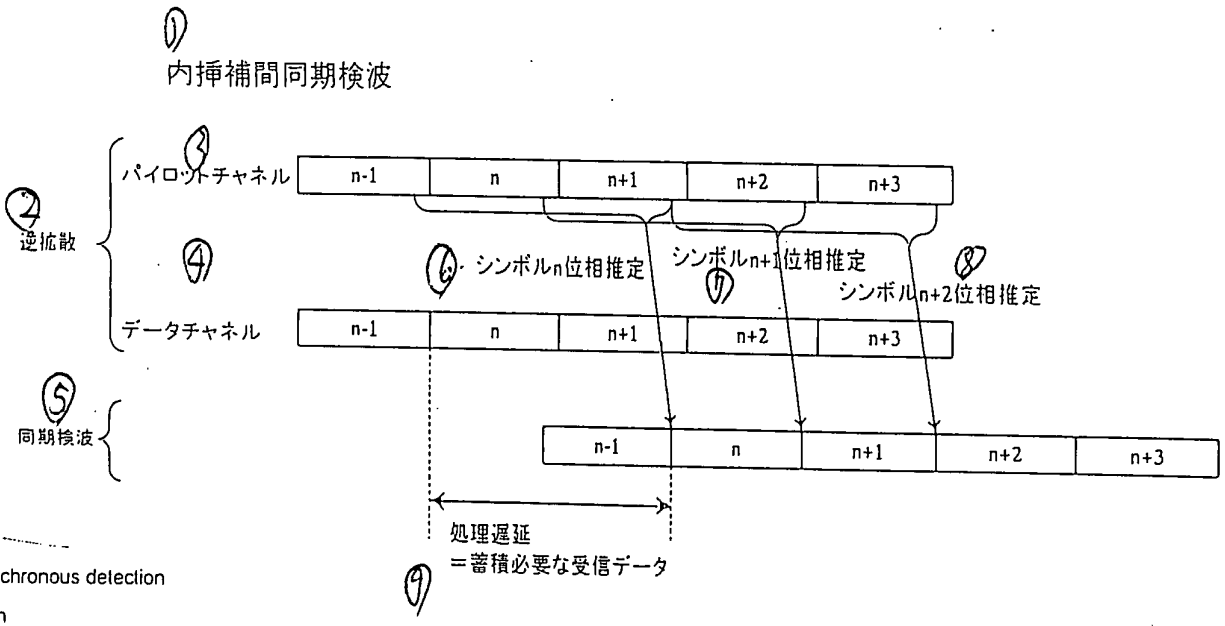


Fig. 29

① Interpolating synchronous detection
② Reverse diffusion
③ Pilot channel
④ Data channel
⑤ Synchronous detection
⑥ Symbol n phase estimation
⑦ Symbol n+1 phase estimation
⑧ Symbol n+2 phase estimation
⑨ Processing delay = receive data required to be stored

Fig. 29

Fig.30

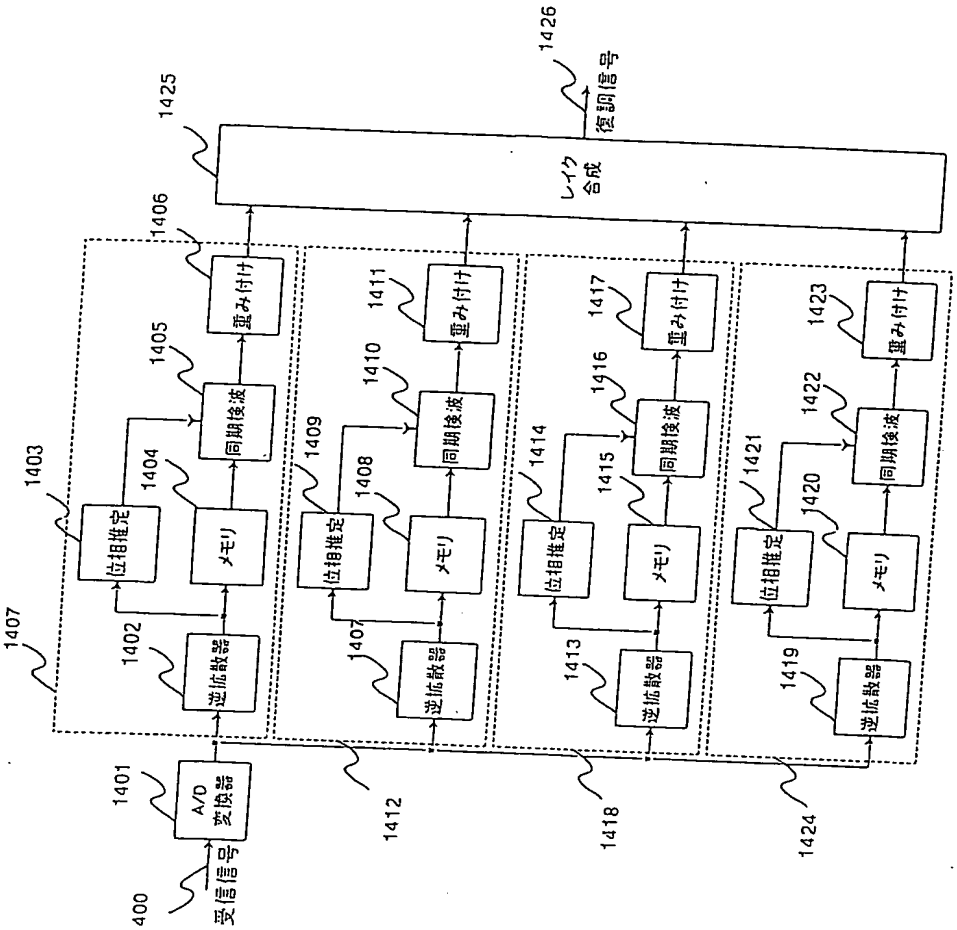
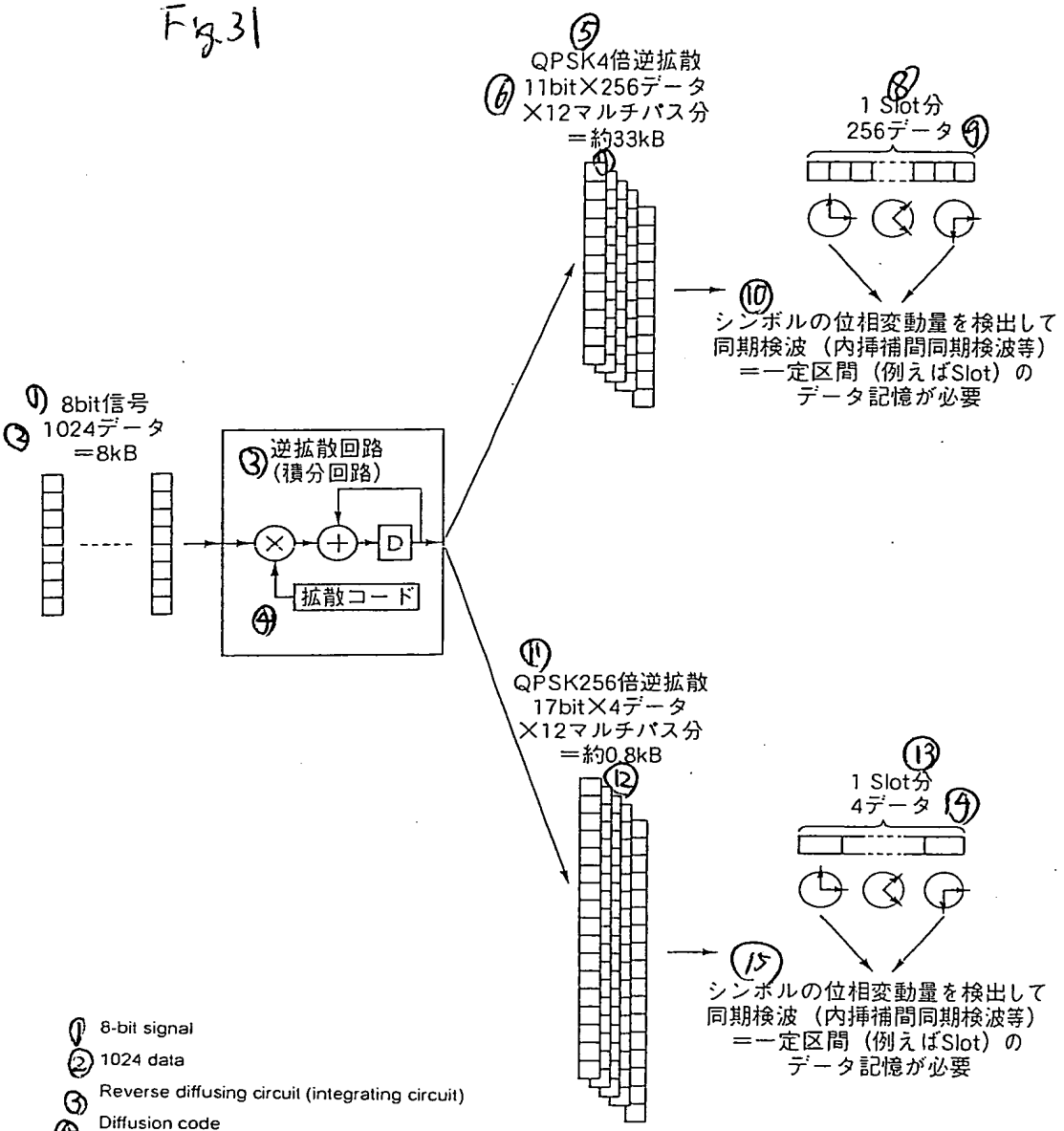


Fig. 30

(1400) receiving signal
(1401) A/D converter
(1402) reverse diffusing unit
(1403) phase estimation
(1404) memory
(1405) synchronous detection
(1406) weighting
(1407) reverse diffusing unit
(1408) memory
(1409) phase estimation
(1410) synchronous detection
(1411) weighting
(1413) reverse diffusing unit
(1414) phase estimation
(1415) memory
(1416) synchronous detection
(1417) weighting
(1419) reverse diffusing unit
(1420) memory
(1421) phase estimation
(1422) synchronous detection
(1423) weighting
(1425) rake synthesis
(1426) demodulating signal

Fig.31



① 8-bit signal

② 1024 data

③ Reverse diffusing circuit (integrating circuit)

④ Diffusion code

⑤ 4-time reverse diffusion

⑥ Portion of 11 bit X 256 data X 12 multipasses

⑦ Approximately

⑧ 1 Slot portion

⑨ Data

⑩ Detect amount of phase fluctuation of symbol and carry out synchronous detection (interpolating synchronous detection) = require storage of data for constant section (for example, Slot)

⑪ Portion of QPSK256-time reverse diffusion 17 bit X 4 data X 12 multipass

⑫ Approximately

⑬ 1 Slot portion

⑭ Data

⑮ Detect amount of phase fluctuation of symbol and carry out synchronous detection (interpolating synchronous detection) = require storage of data for constant section (for example, Slot)